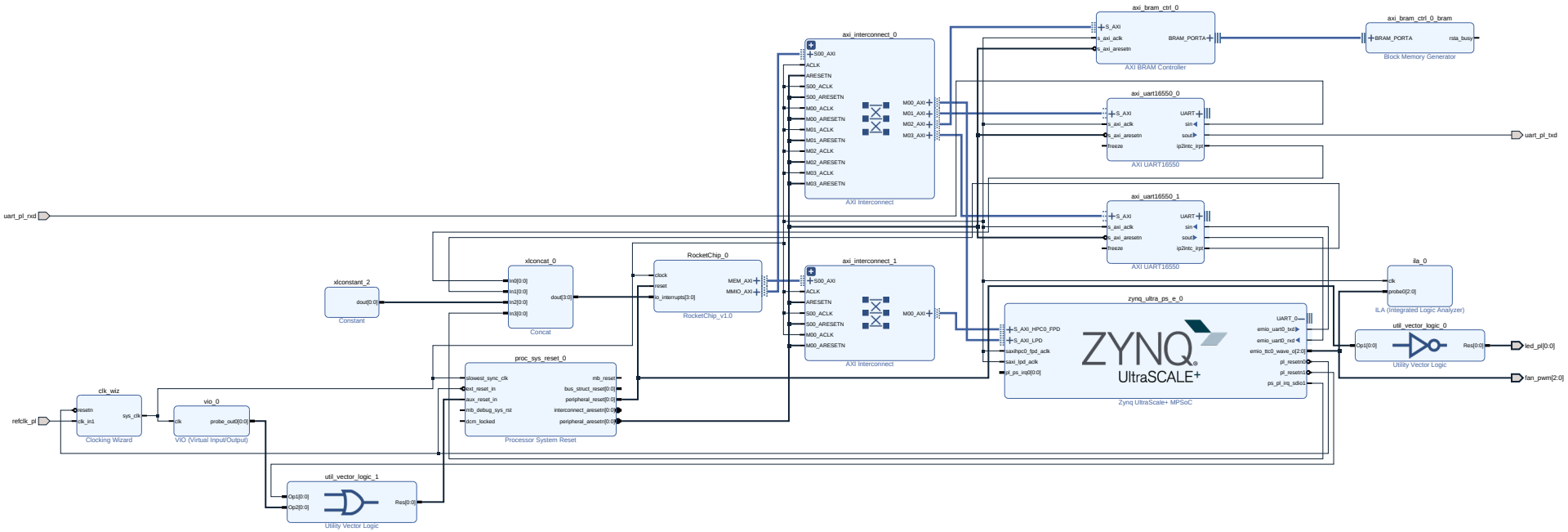
axi_bram_ctrl_0
S_AXI
s_axi_aclk
s_axi_aresetn
BRAM_PORTA
AXI BRAM Controller
axi_bram_ctrl_0_bram
BRAM_PORTA
rsta_busy
Block Memory Generator
axi_interconnect_0
S00_AXI
ACLK
ARESETN
S00_ACLK
S00_ARESETN
M00_ACLK
M00_ARESETN
M01_ACLK
M01_ARESETN
M02_ACLK
M02_ARESETN
M03_ACLK
M03_ARESETN
M00_AXI
M01_AXI
M02_AXI
M03_AXI
AXI Interconnect
axi_uart16550_0
S_AXI
s_axi_aclk
s_axi_aresetn
freeze
UART
sin
sout
ip2intc_irpt
AXI UART16550
uart_pl_txd
uart_pl_rxd
axi_uart16550_1
S_AXI
s_axi_aclk
s_axi_aresetn
freeze
UART
sin
sout
ip2intc_irpt
AXI UART16550
xlconcat_0
in0[0:0]
in1[0:0]
in2[0:0]
in3[0:0]
dout[3:0]
Concat
xlconstant_2
dout[0:0]
Constant
RocketChip_0
clock
reset
io_interrupts[3:0]
MEM_AXI
MMIO_AXI
RocketChip_v1.0
axi_interconnect_1
S00_AXI
ACLK
ARESETN
S00_ACLK
S00_ARESETN
M00_ACLK
M00_ARESETN
M00_AXI
AXI Interconnect
ila_0
clk
probe0[2:0]
ILA (Integrated Logic Analyzer)
zynq_ultra_ps_e_0
S_AXI_HPC0_FPD
S_AXI_LPD
saxihpc0_fpd_aclk
saxi_lpd_aclk
pl_ps_irq0[0:0]
ZYNQ
UltraSCALE+
UART_0
emio_uart0_txd
emio_uart0_rxd
emio_ttc0_wave_o[2:0]
pl_resetn0
pl_resetn1
ps_pl_irq_sdio1
Zynq UltraScale+ MPSoC
util_vector_logic_0
Op1[0:0]
Res[0:0]
Utility Vector Logic
led_pl[0:0]
fan_pwm[2:0]
proc_sys_reset_0
slowest_sync_clk
ext_reset_in
aux_reset_in
mb_debug_sys_rst
dcm_locked
mb_reset
bus_struct_reset[0:0]
peripheral_reset[0:0]
interconnect_aresetn[0:0]
peripheral_aresetn[0:0]
Processor System Reset
clk_wiz
resetn
clk_in1
sys_clk
Clocking Wizard
refclk_pl
vio_0
clk
probe_out0[0:0]
VIO (Virtual Input/Output)
util_vector_logic_1
Op1[0:0]
Op2[0:0]
Res[0:0]
Utility Vector Logic